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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,576	02/12/2004	Toshiharu Furukawa	ROC920030271US1	6152

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EXAMINER
NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/777,576	FURUKAWA ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-13,19,34-42 and 54-58* is/are pending in the application.

4a) Of the above claim(s) *9-13 and 36-42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-8,19,34,35 and 54-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 3, 5-8, 19, 34-35 and 54-58 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the specification for the claimed limitations of said first source/drain contact of said first transistor is aligned with said exterior sidewall of said first gate electrode, and said at least one first semiconducting carbon nanotube is positioned in said dielectric material within said space, and wherein said at least one second semiconducting carbon nanotube is positioned in said dielectric material within said space, and wherein said first source/drain contact of said second transistor is aligned with said vertical exterior sidewall of said second gate electrode, as recited in claims 1, 54 and 58, respectively, because as depicted in figure 9B, said first source/drain contact 50 of said first transistor is NOT aligned with said exterior sidewall of said first gate electrode 25, and said at least one first semiconducting carbon nanotube 42 is NOT positioned in (i.e. within the limits of) said dielectric material 46.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 55-57 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitations of "wherein said first transistor and said second transistor are formed on a substrate, and further comprising: a conductive layer disposed between said first source/drain contact of said first transistor and the substrate", as recited in claim 55, are unclear as to how said first transistor and said second transistor can comprise a conductive layer, wherein said conductive layer is outside the boundaries of said first transistor.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 7-8, 19, 35 and 54-58, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubin et al. (6,933,222).

Regarding claim 1, 3, 7-8, 35, 54 and 58, Dubin et al. teach in figure 5F and related text a device structure comprising:

a first transistor including a first gate electrode 202 with a vertical exterior sidewall (said sidewall is the most extreme right sidewall of gate electrode 202 which is in direct contact with the gate dielectric to which reference number 202 is pointing to), a first gate dielectric 215 disposed on the vertical exterior sidewall of said first gate electrode, at least one first a semiconducting carbon nanotube 250a having a first end, a second end, and a channel region between said first and second ends and disposed adjacent to said vertical exterior sidewall of said first gate electrode, a first source/drain contact 222 electrically coupled with said first end of said at least one first semiconducting carbon nanotube, and a second source/drain contact 224 electrically coupled with said second end of said at least one first semiconducting carbon nanotube; a second transistor including a second gate electrode 202 with a vertical exterior sidewall, a second gate dielectric 215 disposed on the vertical exterior sidewall of said second gate electrode, at least one second semiconducting carbon nanotube 250b having a first end, a second end, and a channel region between said first and second ends and disposed adjacent to said vertical exterior sidewall of said second gate electrode, a third source/drain contact 222 electrically coupled with said first end of said at least one second semiconducting carbon nanotube, and a fourth source/drain contact 224 electrically coupled with said second end of said at least one second semiconducting carbon nanotube, said vertical exterior sidewall of said second gate

electrode separated from said vertical exterior sidewall of said first gate electrode by a space; and

a layer 216 composed of a dielectric material and disposed in said space, and

said at least one first semiconducting carbon nanotube is positioned in said dielectric material within said space.

wherein each of said at least one first semiconducting carbon nanotube is a single-wall semiconducting carbon nanotube,

wherein said first transistor further comprises: an insulating layer 214 disposed between said first source/drain contact and said first gate electrode for electrically isolating said first contact from said first gate electrode,

wherein said first transistor further comprises: an insulating layer 215, 216 disposed between said second source/drain contact and said first gate electrode for electrically isolating said second source/drain contact from said first gate electrode, and

a capacitor electrically coupled with said first source/drain contact,

wherein said at least one second semiconducting carbon nanotube is positioned in said dielectric material within said space.

Dubin et al. do not teach said first source/drain contact of said first/second transistor is aligned with said exterior sidewall of said first/second gate electrode.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a first source/drain contact of said first/second transistor to be aligned with said exterior sidewall of said first/second gate electrode in prior art's device in order to simplify the processing steps of making the device.

Regarding claim 19, Dubin et al. teach substantially the entire claimed structure, as applied to claim 1 above, including a substrate 210 carrying said first and second transistors and characterized by a surface area viewed vertical to the substrate. Dubin et al. do not state that said dielectric-filled space ranges from about 20 percent to about 50 percent of said surface area.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a space ranging from about 20 percent to about 50 percent of said surface area in prior art's device in order to reduce the size of the device (by providing a space ranging only from about 20 percent to about 50 percent of the total surface area) and by optimizing the characteristics of the device (by not proving the structures too close to each other which may degrade the device performance).

Regarding claims 55 and 56, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a conductive layer disposed between said first source/drain contact of said first/second transistor and the substrate in prior art's device, in order to operate the device by providing electrical connection to the first source/drain contact of said first/second transistor.

Regarding claim 57, it would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose an insulating layer between said first gate electrode and said conductive layer in prior art's device, in order to not to short circuit the device.

Claims 5-6 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubin et al. in view of Farnworth et al. (6,515,325).

Regarding claims 5 and 34, Dubin et al. teach substantially the entire claimed structure, as applied to claim 1 above, except explicitly stating that said first source/drain contact includes a catalyst pad characterized by nanocrystals of a catalyst material effective for growing said at least one semiconducting carbon nanotube.

Farnworth et al. teach in figure 2A and related text (column 4, lines 32-50) a first contact includes a catalyst pad (by considering the first contact layer as layer 16, the catalyst pad is layer 16) characterized by nanocrystals of a catalyst material effective for growing said at least one semiconducting carbon nanotube.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first contact in prior art's device by including a catalyst pad characterized by nanocrystals of a catalyst material effective for growing said at least one semiconducting carbon nanotube, in order to simplify the processing steps of making the device by using conventional growing method of semiconducting carbon nanotube.

Regarding claim 6, prior art's device includes said first end of said at least one semiconducting carbon nanotube has a composition including the catalyst material or a material alloyed with the catalyst material.

Regarding the process limitations recited in claims 5 and 34 ("nanocrystals of a catalyst material effective for growing said at least one semiconducting carbon nanotube", and "an electrical-conductivity enhancing substance diffused from said catalyst pad into said first end during growth"), these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Response to Arguments

Applicant argues that Dubin et al. do not teach the claimed limitation of said vertical exterior sidewall of said second gate electrode separated from said vertical exterior sidewall of said first gate electrode by a space; and a layer composed of a dielectric material and disposed in said space, wherein said at least one first semiconducting carbon nanotube is positioned in said dielectric material within said

space, because according to the reproduced figure 5E of Dubin et al., by applicant, the nanotubes are not located between the vertical exterior sidewall of said second gate electrode and the vertical exterior sidewall of said first gate electrode.

Applicant arbitrarily choose the vertical exterior sidewall of said second gate electrode and the vertical exterior sidewall of said first gate electrode to be the sidewalls located to the extreme left side and the extreme right side of the respective transistors. However, by choosing the vertical exterior sidewall of said second gate electrode and the vertical exterior sidewall of said first gate electrode to be the sidewalls located to the extreme right side and the extreme left side of the respective transistors, such that both nanotubes are located between the two sidewalls, then the claimed limitations are met.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
2/16/2010

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